

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-4. (Cancelled)

5. (Previously Presented) The method for forming a semiconductor device according to claim 16, in which said step f1) comprises:

depositing said second insulating film using a TEOS-CVD method utilizing TEOS activated by O₃.

6.-10. (Cancelled)

11. (Previously Presented) The method for forming a semiconductor device according to claim 16, wherein said upper layer is an Al layer.

12. (Previously Presented) The method for forming a semiconductor device according to claim 11, wherein

said step of depositing said Al layer comprises sputtering while heating said circuit board in a temperature range of 100 to 400°C.

13. (Cancelled)

14. (Previously Presented) The method for forming a semiconductor device according to claim 16, wherein

said step of forming said surface protective film comprises depositing SiN through a plasma-excitation CVD method having an RF power of 300 W or less.

15. (Cancelled)

16. (Previously Presented) A method for forming a semiconductor device, comprising the steps of:

a) providing a circuit board;

- b) forming a first insulating film at least indirectly on said circuit board;
 - c) forming a lower electrode on said first insulating film;
 - d) forming a ferroelectric film over said lower electrode;
 - e) forming an upper electrode over said ferroelectric film, said lower electrode, ferroelectric film, and said upper electrode combining to form a ferroelectric capacitor;
 - f) creating a synthetic tensile stress upon said ferroelectric capacitor by:
 - f1) forming a second insulating film over said ferroelectric capacitor;
 - f2) forming a metal wiring film over said second insulating film; and
 - f3) forming a surface protective film over said second insulating film and said metal wiring film;
- in which step f2) comprises forming the metal wiring film by:
- f2a) depositing a TiN layer as a lower metal layer;
 - f2b) heat-treating said TiN layer to create a tensile stress; and
 - f2c) depositing an upper metal layer directly on said TiN layer over said ferroelectric capacitor.

17. (Previously Presented) The method as in claim 16, in which step f2b) comprises heat-treating said TiN layer in a temperature range of 200 to 650°C.

18. (Previously Presented) The method as in claim 17, in which in step f2b) said stress in said TiN layer changes from a compression-directional stress to an extensional directional stress.

19. (Previously Presented) The method as in claim 16, in which in step f2b) said stress in said TiN layer changes from a compression-directional stress to an extensional directional stress.

20. (Previously Presented) The method of claim 16, in which:

step f1) comprises depositing said second insulating film using a TEOS-CVD method utilizing TEOS activated by O_3 ;

step f2b) comprises heat-treating said TiN layer in a temperature range of 200 to 650°C;

said upper layer is an Al layer. and said step of depositing said Al layer comprises sputtering while heating said circuit board in a temperature range of 100 to 400°C; and

said step of forming said surface protective film comprises depositing SiN through a plasma-excitation CVD method having an RF power of 300 W or less.

21. (Previously Presented) The method as in claim 20, in which in step f2b) said stress in said TiN layer changes from a compression-directional stress to an extensional directional stress.